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The HP AutoRAID hierarchical storage system

J. Wilkes, R. Golding, C. Staelin, T. Sullivan

December 1995 ACM SIGOPS Operating Systems Review, Proceedings of the fifteenth ACM symposium on Operating systems principles, Volume 29 Issue 5

Full text available: pdf(1.60 MB)

Additional Information: full citation, references, citings, index terms

High-performance raster graphics for microcomputer systems

Andreas Bechtolsheim, Forest Baskett

July 1980 ACM SIGGRAPH Computer Graphics, Proceedings of the 7th annual conference on Computer graphics and interactive techniques, Volume 14 Issue 3

Full text available: pdf(424.75 KB) Additional Information: full citation, abstract, references, index terms

A frame buffer architecture is presented that reduces the overhead of frame buffer updating by three means. First, the bit-map memory is (x,y) addressable, whereby a string of pixels can be accessed in parallel. Second, the pixel-change operation is performed by hardware in a single read-modify-write cycle. Third, multiple objects in the frame buffer are addressable simultaneously by a set of address registers. The remaining task of generating (x,y)addresses and providing new data can be m ...

Keywords: Bit-map, Frame buffer, Functional memory, Raster operation, Raster-scan graphics

The HP AutoRAID hierarchical storage system

John Wilkes, Richard Golding, Carl Staelin, Tim Sullivan February 1996 ACM Transactions on Computer Systems (TOCS), Volume 14 Issue 1

Full text available: pdf(1.82 MB)

Additional Information: full citation, abstract, references, citings, index terms

Configuring redundant disk arrays is a black art. To configure an array properly, a system administrator must understand the details of both the array and the workload it will support. Incorrect understanding of either, or changes in the workload over time, can lead to poor performance. We present a solution to this problem: a two-level storage hierarchy implemented inside a single disk-array controller. In the upper level of this hierarchy, two copies of active data are stored to provide f ...

Keywords: RAID, disk array, storage hierarchy



Hardware fault containment in scalable shared-memory multiprocessors

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StarT-Voyager: a flexible platform for exploring scalable SMP issues

Boon S. Ang, Derek Chiou, Daniel L. Rosenband, Mike Ehrlich, Larry Rudolph, Arvind November 1998 Proceedings of the 1998 ACM/IEEE conference on Supercomputing (CDROM)

Full text available: (a) html(49.51 KB) Additional Information: full citation, abstract, references, citings

This paper describes StarT-Voyager, a machine designed as an experimental platform for research in cluster system communication. The heart of StarT-Voyager is a network interface unit (NIU) that connects the memory bus of a PowerPC-based SMP to the MIT Arctic network. The NIU is highly flexible, with its set of functions easily modified by firmware or by programmable hardware, making it possible to compare different communication interfaces and implementation strategies on a common platform. Its ...

Keywords: configurable hardware, flexible, message passing, network interface unit, parallel systems, shared memory

Macintosh OS X: a smooth migration

Scott E. Hanselman, Mahmoud Pegah

September 2003 Proceedings of the 31st annual ACM SIGUCCS conference on User services

Full text available: 🔂 pdf(208.81 KB) Additional Information: full citation, abstract, references, index terms

The Ringling School of Art and Design is a fully accredited four year college of visual art and design with a student population of approximately 1000. The Ringling School has achieved national recognition for its large-scale integration of technology into collegiate visual art and design education and maintains a student to computer ratio of better than two to one. Due to the demand for computing power and the requirement for ease of use, we moved our instructional computer laboratories to the ...

Keywords: Macintosh OS X, NFS, NIS, SSH, fonts, migration, network

3 Pen computing: a technology overview and a vision

André Mever

July 1995 ACM SIGCHI Bulletin, Volume 27 Issue 3

Full text available: pdf(5.14 MB) Additional Information: full citation, abstract, citings, index terms

This work gives an overview of a new technology that is attracting growing interest in public as well as in the computer industry itself. The visible difference from other technologies is in the use of a pen or pencil as the primary means of interaction between a user and a machine, picking up the familiar pen and paper interface metaphor. From this follows a set

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1 Design and implementation of the POWER5/spl trade/ microprocessor

Clabes, J.; Friedrich, J.; Sweet, M.; DiLullo, J.; Chu, S.; Plass, D.; Dawson, J.; Muench, P.; Powell, L.; Floyd, M.; Sinharoy, B.; Lee, M.; Goulet, M.; Wagoner, J.; Schwartz, N.; Runyon, S.; Gorman, G.; Restle, P.; Kalla, R.; McGill, J.; Dodson, S.; Integrated Circuit Design and Technology, 2004. ICICDT '04. International Conference on , 2004

Pages: 143 - 145

[Abstract] [PDF Full-Text (333 KB)]

2 Simultaneous subordinate microthreading (SSMT)

Chappell, R.S.; Stark, J.; Kim, S.P.; Reinhardt, S.K.; Patt, Y.N.; Computer Architecture, 1999. Proceedings of the 26th International Symposium on, 2-4 May 1999

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